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Effect of Si Interface Surface Roughness To The Tunneling Current of The Si/Si_{1-x}Ge_x/Si Heterojunction Bipolar Transistor

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Abstract. In this work we discuss the surface roughness of Si interface impact to the tunneling current of the Si/Si_{1-x}Ge_x/Si heterojunction bipolar transistor. The Si interface surface roughness can be analyzed from electrical characteristics through the transversal electron velocity obtained as fitting parameter factor. The results showed that surface roughness increase as Ge content of virtual substrate increase This model can be used to investigate the effect of Ge content of the virtual substrate to the interface surface condition through current-voltage characteristic.

INTRODUCTION

SiGe heterostructure has a high ability to improve the Si devices. Currently the application of SiGe heterojunction bipolar transistors is grow more popular in wireless and high-speed digital communication. Advantage of SiGe heterojunction bipolar transistor from the Ge integration into base which results in bandgap reduction and enhance in intrinsic carrier concentration in base region primary to increased emitter injection efficiency. Besides that, the semiconductor structure has to be improved by semiconductor-based heterostructure. The arrowhead of the heterostructure is given by silicon germanium (SiGe)/silicon interface junctions. The spread of commercially available devices with SiGe/Si heterostructures started with the introduction of hetero bipolar transistor (HBT) devices which has been proven a tremendous speed advantages in bipolar and BiCMOS circuits¹.

Producing an abrupt Si/SiGe interface is a serious problem involve in ideal Si/SiGe heterostructure formation. Many problems have to be overcome in high quality Si and SiGe layers with perfectly flat and abrupt interfaces without noticeable intermixing. One of the challenges for globally strained Si/SiGe is material quality since epitaxial growth of strained layers on relaxed virtual substrate leads to surface roughness^{2,3}. Si grown on SiGe virtual substrate will meets an interfacial mixing because of the surface segregation of Ge atoms. Ge atoms will diffuse into Si layer make Si interface surface become roughness and not abrupt. It will disrupt the electrons motion in the Si surface influences the electrical properties of the devices⁴. Segregation in the epitaxial growth of Si on Ge/Si (001) mechanism and physically-based model of diffusion in SiGe has been observed⁵.

Due to the small transistor size, the electron transport becomes more ballistic. The effect of coupling between the transversal and the longitudinal components of electron motion, which obtained from the Schrödinger equation solution, cannot be ignored for electrons with high phase velocity⁶. However, these studies have not dealt with the influence of the interface surface condition to the electrical characteristic.

In this paper we present the influence of the Si interface surface roughness to the Si/Si_{1-x}Ge_x/Si heterojunction bipolar transistor collector current. We performed fitting of the analytical tunneling current calculation to the published experiment data. The Si interface surface can be analyzed from the transversal electron velocity value. From here, we can understand the effect of Ge content of the Si_{1-x}Ge_x alloy to the Si surface roughness.

THEORETICAL METHOD

The unstrained SiGe layers grown on Si substrates called as “virtual substrates”. Due to the 4.2 % mismatch in lattice spacing of Si and Ge atoms, tensile strain in Si can be generated through epitaxial growth of Si on a relaxed SiGe virtual substrate⁷. When Si layers are grown on SiGe virtual substrate and are under lateral tensile strain, type-II (Fig.1) alignment is realized and electrons and holes are separately confined⁸.

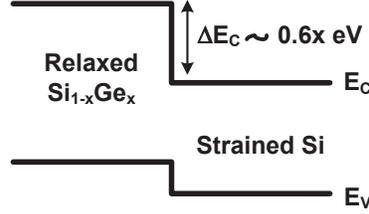


FIGURE 1. Band alignment between Si and Si_{1-x}Ge_x on Si_{1-x}Ge_x virtual substrate.

The key to SiGe heterojunction bipolar technology progress has been establishment in epitaxial systems that have permissible the growth of pseudomorphic (strained) Si_{1-x}Ge_x. Pseudomorphic Si_{1-x}Ge_x has bandgap smaller than Si which will provide a reduction in the potential barrier to electrons in the emitter. The results are an increased collector current and accordingly enhanced gain.

Electron in Si/Si_{1-x}Ge_x/Si structure is moving in anisotropic heterostructure. The strain caused by the pseudomorphic growth of the epilayers results in strong band structure anisotropy. Besides that, Si and SiGe are indirect semiconductor materials so they must be treated as anisotropic material.

The behavior of an electron in anisotropic materials is under the parabolic-band effective mass approximation. We will obtain the Schrödinger-like equation in the base region as⁶

$$\left[-\frac{\hbar^2}{2m_0} \alpha_{ij} \frac{d^2}{dz^2} + \left(\Phi - \frac{\hbar^2}{2m_0} \sum_{i,j} \beta_{ij} k_i k_j \left(1 - \frac{\beta_{ij}}{\beta_{0i}} \right) \right) \right] \varphi(z) = E \varphi(z) \quad (1)$$

where \hbar is the reduced Planck constant, m_0 is the mass of free electrons, α is the inverse effective-mass tensor, β contain of α , Φ is conduction band discontinuity, k_i is wavenumbers, E is the total energy and φ is the wavefunction.

Identifying $\langle E \rangle$ as the average kinetic energy of electron in the emitter region, where v_p is the phase velocity of electrons in the direction parallel to the Si/SiGe interface. Eq. (1) creates the coupling between longitudinal (perpendicular to the interface) and transversal (parallel to the interface) kinetic energies of the electron motion in the anisotropic heterostructure.

Solution of the Schrödinger equation above will give an electron probability to tunnel the Si_{1-x}Ge_x barrier. This electron transmittance then used to calculate the electron tunneling current density⁹.

This was known since long ago that the Si growth over Ge layers suffers from an interfacial mixing. Ge will segregate when forming Si strained layers on SiGe relaxed virtual substrate during epitaxial growth. Ge out diffusion from a SiGe virtual substrate during high thermal processing can degrade Si/SiGe interface quality. It make the real hetero-interface is not atomically flat and abrupt. This is because the Ge atoms have different structure and form with Si. Surface segregation is one of the cause deteriorate interface abruptness in the Si/SiGe interface. Atomic scale segregation processes can profoundly influence the electronic properties of SiGe alloys¹⁰. Ge diffusion will yield electron motion on the Si layer upset.

RESULTS AND DISCUSSION

We made comparison between the data calculated with published experiment for Ge content 20% and 30% of SiGe (110) virtual substrate. The conduction band discontinuity was taken as 91.5 and 133 meV for Ge content 20% and 30%, respectively. The effective masses of Si_{0.8}Ge_{0.2} and Si_{0.7}Ge_{0.3} used in this calculation are shown in Table 1 and 2, respectively. Calculation done for V_{BE} value varied between 0.2 – 1 V and V_{BC} fix at 0 V. V_{BE} is forward bias voltage of base–emitter junction and V_{BC} is reverse biased voltage of base–collector junction. The SiGe thickness and temperature, are 20 nm and 300 K, respectively. Here, the tunneling current calculations were applied for tensile

strain because electron transport more dominant at tensile than compressive strain¹¹. Fitting parameter of this comparison was the electron velocity in the transversal motion. The transversal electron velocity is the velocity in the direction of motion parallel to the Si interface. This will be strongly influenced by the state of the Si interface surface.

Table 1 . Tensor elements α_{ij} of Si(110) and $\text{Si}_{0,8}\text{Ge}_{0,2}$

Valley	Si(110)			$\text{Si}_{0,8}\text{Ge}_{0,2}$		
1 (L1)	5,26	0	0	5,68	0	0
	0	3,14	2,12	0	3,51	2,31
	0	2,12	3,14	0	2,31	3,51
2 (L2)	5,26	0	0	5,68	0	0
	0	3,14	-2,12	0	3,51	-2,31
	0	-2,12	3,14	0	-2,31	3,51
3 (L3)	1,09	0	0	0,90	0	0
	0	5,26	0	0	5,68	0
	0	0	5,26	0	0	5,68

Table 2 . Tensor elements α_{ij} of Si(110) and $\text{Si}_{0,7}\text{Ge}_{0,3}$

Valley	Si(110)			$\text{Si}_{0,7}\text{Ge}_{0,3}$		
1 (L1)	5,26	0	0	5,91	0	0
	0	3,14	2,12	0	3,86	2,45
	0	2,12	3,14	0	2,45	3,86
2 (L2)	5,26	0	0	5,91	0	0
	0	3,14	-2,12	0	3,86	-2,45
	0	-2,12	3,14	0	-2,45	3,86
3 (L3)	1,09	0	0	0,85	0	0
	0	5,26	0	0	5,91	0
	0	0	5,26	0	0	5,91

Fig. 2 shows comparison between the calculation (symbols) and experiment (line)¹² of tunneling currents. The tunneling currents value is the same for both calculation and experimental only when V_{BE} is below 0.6 V. The deviation is assumed to be caused by negligence on the depletion region at emitter-base boundary¹³. Comparison between the data calculated with measuring produces the electron velocity for $\text{Si}_{0,7}\text{Ge}_{0,3}$ and $\text{Si}_{0,8}\text{Ge}_{0,2}$ are 11.2×10^5 m/s dan 16.7×10^5 m/s, respectively. The electron velocity increases as the Ge content decrease can be explained by this reason. Crystallographic quality of the (110) and (111) strain-Si layers seems to decrease when Ge content of SiGe virtual substrate are higher¹⁴. It is happen because of dislocation in the form of surface roughness as the Ge content virtual substrate increased. Ge outdiffusion from SiGe virtual substrate will enter into Si surface. Surface roughness plays important role on the transistor electrical properties such as electronic conductivity because its will disturbed electrons motion in the Si/SiGe interface. As the Ge content virtual substrate increase the surface roughness Si parallel to SiGe virtual substrate interface will increase. So it makes the electron velocity in transversal motion will decrease. From law energy conservation, the longitudinal energy of electron will increase as the transversal energy decrease. Therefore, the effective $\text{Si}_{1-x}\text{Ge}_x$ barrier potential will decrease as the Ge content virtual substrate increased. This will cause the tunneling currents increase as the Ge content virtual substrate increased. The collector current, for Ge content of 20%, at V_{BE} above 0.6 V is investigated by comparing it with the fullband Monte Carlo (MC) simulation⁹. The electron velocity that used for fitting with MC simulation is the same as before and the result obtained is similar until V_{BE} below 0.8 V.

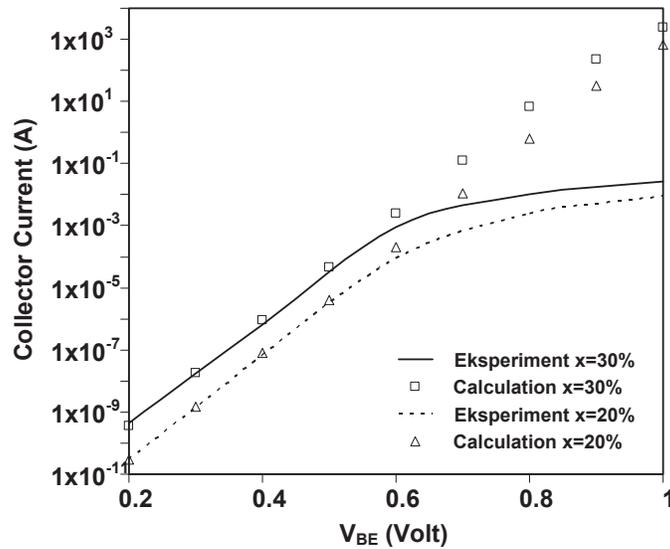


FIGURE 2. Collector characteristic of the Si(110)/Si_{1-x}Ge_x(110)/Si(110) heterojunction bipolar transistor with Ge concentration x 30 % and 20 % and emitter area 30x30 μm^2 .

CONCLUSIONS

The relation between electrical characteristic with Si interface quality had been investigated. The transversal electron velocity, which was obtained from calculation data that had been fitted to experiment result, showed silicon surface layer condition. Fitting result with experiment data, for vary Ge content, agreed only for voltage V_{BE} below 0.6 V, but above 0.6 V this model follows the Monte Carlo model. It can be seen that surface roughness will increase as Ge content of virtual substrate increase. This model can show how the current-voltage characteristic associated with the Si interface surface condition.

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